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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,130	12/30/2003	Alessia Pavan	2110-99-3	3296

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GRAYBEAL, JACKSON, HALEY LLP
155 - 108TH AVENUE NE
SUITE 350
BELLEVUE, WA 98004-5901

EXAMINER	
FARAHANI, DANA	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,130	PAVAN ET AL.	
	Examiner	Art Unit	
	Dana Farahani	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5-24-04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable Nakajima et al., hereinafter Nakajima (US Patent 5,614,748) in view of Catabay et al., hereinafter Catabay (US Patent 6,800,940), all previously cited.

Regarding claims 1, 4, and 6, Nakajima discloses in figure 1, a non-volatile memory comprising:

a floating gate transistor including a source region 24b and a drain region 24a, a gate region projecting from the substrate and comprised between said source and drain regions, said gate region having a predetermined length and width and comprising a first floating gate region 8 and a control gate region 12, characterized in that said floating gate region is insulated laterally, along the width direction, by a dielectric layer 14 with a dielectric constant value.

Nakajima does not disclose the low dielectric constant value is between 1 and 3.9 (low dielectric), and the layer is formed by an oxide layer, hydrated with alkylic groups.

Catabay discloses in figure 4, and column 6, lines 23-37, a carbon doped silicon layer 30 in the integrated circuit structure shown. Catabay further discloses this kind of layer is void free and have a dielectric constant of less than 3 (see column 4, lines 35-40 and 52-55), further disclosing low dielectric constant values reduces horizontal capacitance between conductive

lines (see column 2, lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use carbon doped oxide layer in the structure of Nakajima to benefit from the advantageous properties of the layer such as reduced capacitance between the gate electrodes. Note that using alkylic groups to dope the oxide layer is a method of doping the oxide layer.

Regarding claim 2, the floating gate regions are covered by a dielectric layer 30a before being insulated from each other through said dielectric layer with low dielectric constant value (see figure 3D).

Regarding claim 3, the dielectric layer with low dielectric constant value is bounded between said floating gate regions, as can clearly be seen in figure 1.

3. Claims 15-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima in view of Catabay and further in view of Lee et al., hereinafter Lee (US Patent 6,717,846), previously cited.

Regarding claims 15, 16, 18, 21, 24, and 25, Nakajima in view of Catabay substantially discloses the limitations in the claims, as discussed above, except for expressly stating the cells are organized in a matrix form.

Lee discloses memory cells are arranged in rows and column (figure 2a) to make a memory array. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the memory cell of the Nakajima reference in a matrix form, since memory cells are normally arranged in a matrix pattern to make them usable in various applications.

Regarding claims 17 and 23, the memory cell of Nakajima has an ONO dielectric layer 10 having a greater dielectric constant than the insulating regions formed on the floating gate regions.

Regarding claims 19, 20, 22, and 26, note that the gates of the transistors in the Lee reference are connected to each other and the cells are flash memory cells. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the memory cell of the structure of Nakajima in view of Catabay in a storage memory matrix form with the gates of the cells connected, to take advantage of the benefits the cell offers, such as low leakage current (see Nakajima, column 1, lines 60-67).

Response to Arguments

4. Applicants' arguments filed on 12/30/05 have been fully considered but they are not persuasive.

Applicants' argument that the Nakajima reference shows a memory cell in the length direction and not width direction, since there is no explicit definition of the intended use of the word "width" in the specification, one of ordinary skill in the art could call the cross section view of the Nakajima reference width direction, from top to the bottom, in which case the floating gate regions are insulated laterally along the width direction. Assuming, arguendo, that the width direction is defined as same as applicants' intended use of the word, the floating gates are still insulated laterally along the width direction, as shown in figure 2 (insulating film 14 is formed in between the floating gates along a width direction). Assuming that non of the above scenarios is the case, while the Office does not agree with this assumption, the secondary reference cited,

catabay, shows that there is a problem of capacitance between adjacent conductive lines, and therefore, one of ordinary skill in the art would have been motivated to include the insulator layer 14 of the Nakajima reference along the width direction, the meaning of which is the meaning intended by applicants, to prevent capacitive coupling between the floating gates.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800